Please add the following new claims:

SUB C2 -- 12. (New) A high-voltage MOS transistor wherein a dopant concentration of a source offset region is set lower that a dopant concentration of a drain offset region such that the following inequality is not [easily satisfied]: ≤ ← in the spec.

VW – (a forward biased breakdown voltage of silicon) [>] VS

figs. 4, 10(a) p. 32-33

where, VW is a substrate voltage of a substrate region directly under a gate insulating film, and VS is a source voltage of the source offset region, and thereby a resistance value of the source offset region is set independently of a resistance value of the drain offset region in such a manner as to maintain a high sustaining breakdown voltage of the high-voltage MOS transistor, which is based on a voltage of the source offset region and a voltage of the substrate region directly under a gate insulating film during operation of the high-voltage MOS transistor.

B2

13. (New) A high-voltage MOS transistor wherein a length of a region overlapping between a source offset region and a source well offset region is set smaller than a length of a region overlapping between a drain offset region and a drain well offset region and thereby a resistance value of source offset region is set independently of a resistance value of the drain offset region in such a manner as to maintain a high-sustaining breakdown voltage of the high-voltage MOS transistor, which is based on a voltage of the source offset region and a voltage of a substrate region directly under a gate insulating film during operation of the high-voltage MOS transistor.

figs. 1, 7

14. (New) A high-voltage MOS transistor wherein a length of a region overlapping between a source offset region and a source well offset region is set smaller than a length of a region overlapping between a drain offset region and a drain well offset region such that the following inequality is not [easily satisfied]: